

**Features:**

- Isolated mounting base 4000V~
 - Pressure contact technology with Increased power cycling capability
 - Space and weight saving
- Typical Applications**
- AC/DC Motor drives
 - Various rectifiers
 - DC supply for PWM inverter

V_{DSM}, V_{RSM}	V_{DRM}, V_{RRM}	Type & Outline
2700V	2600V	MFx800-26-410F3
2900V	2800V	MFx800-28-410F3
3100V	3000V	MFx800-30-410F3
3300V	3200V	MFx800-32-410F3
3500V	3400V	MFx800-34-410F3
3700V	3600V	MFx800-36-410F3

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_J(^{\circ}C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, $T_c=85^{\circ}C$	125			800	A
$I_{T(RMS)}$	RMS on-state current					1256	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			55	mA
I_{TSM}	Surge on-state current	10ms half sine wave $V_R=60\%V_{RRM}$	125			14.5	kA
I^2t	I^2t for fusing coordination					1051	$A^2s \times 10^3$
V_{TO}	Threshold voltage		125			0.85	V
r_T	On-state slope resistance					0.19	mΩ
V_{TM}	Peak on-state voltage	$I_{TM}=2400A$	25			2.80	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=67\%V_{DRM}$	125			800	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A $t_r \leq 0.5\mu s$ Repetitive	125			100	A/μs
I_{GT}	Gate trigger current	$V_A=12V, I_A=1A$	25	30		200	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			10		200	mA
V_{GD}	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.041	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.024	°C /W
V_{iso}	Isolation voltage	50Hz, R.M.S, $t=1min, I_{iso}:1mA(MAX)$		4000			V
F_m	Terminal connection torque(M12)				14.0		N·m
	Mounting torque(M8)				12.0		N·m
T_{vj}	Junction temperature			-40		125	°C
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				3240		g
Outline	410F3						

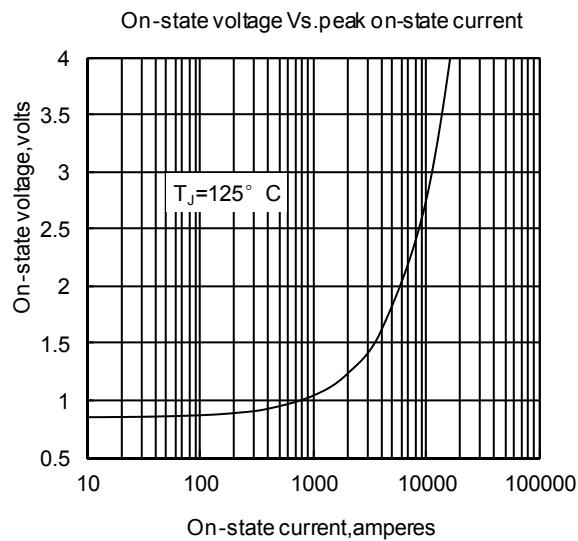


Fig. 1

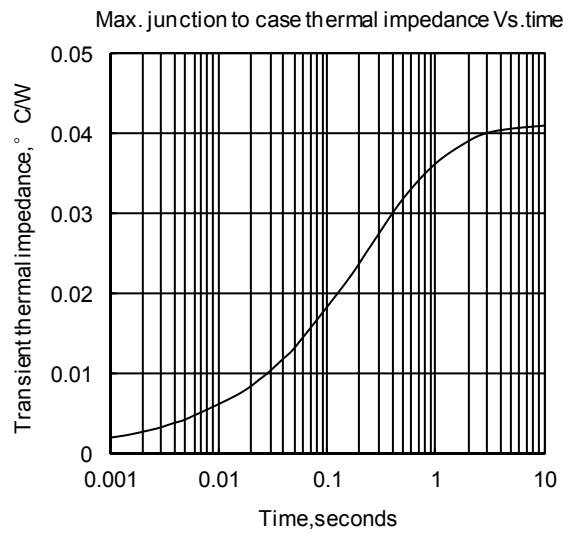


Fig. 2

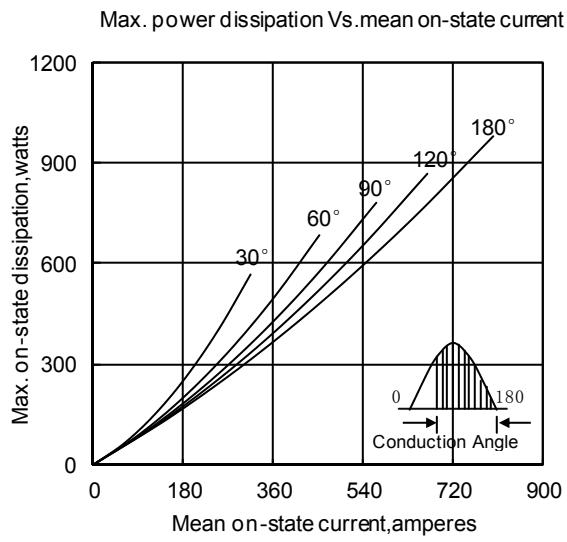


Fig. 3

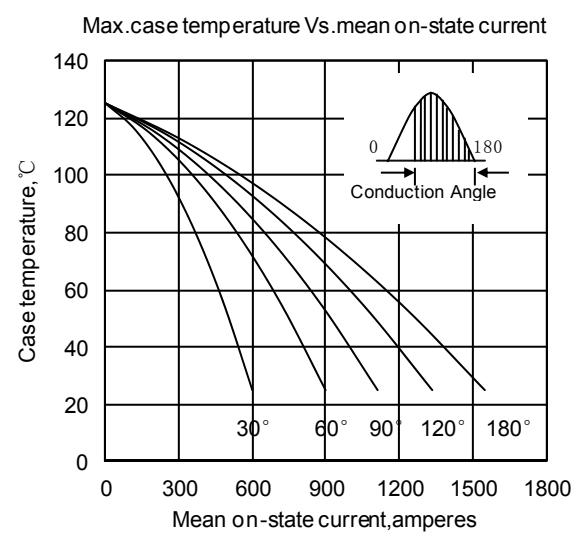


Fig. 4

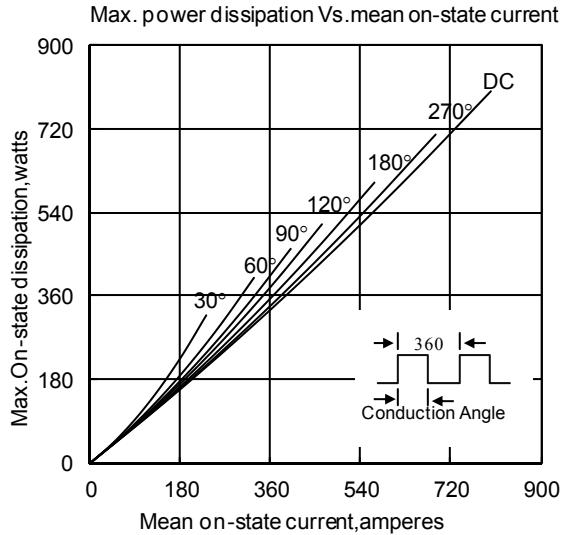


Fig. 5

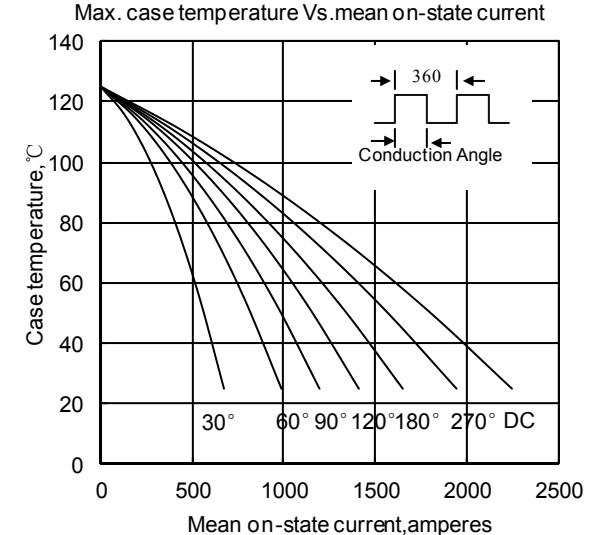


Fig. 6

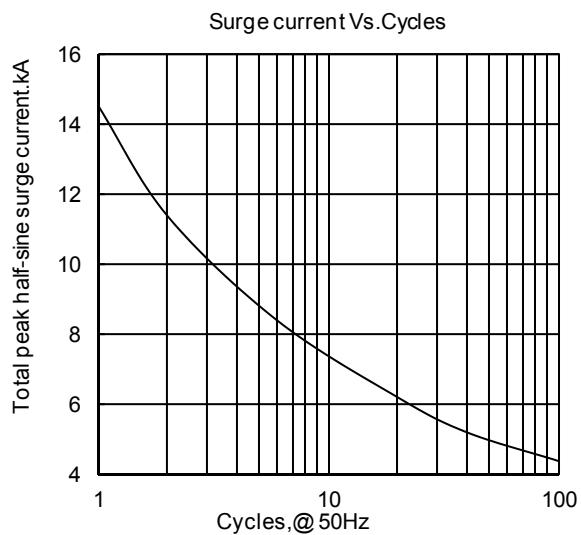


Fig. 7

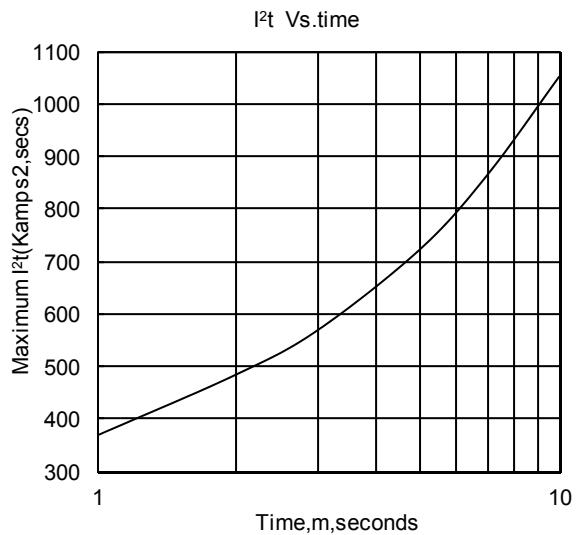


Fig. 8

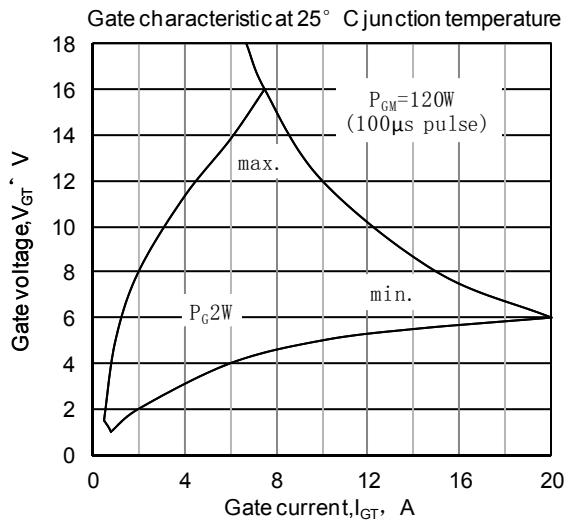


Fig. 9

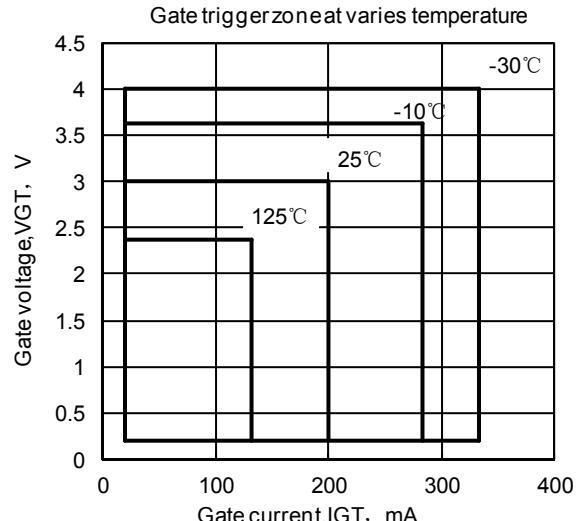
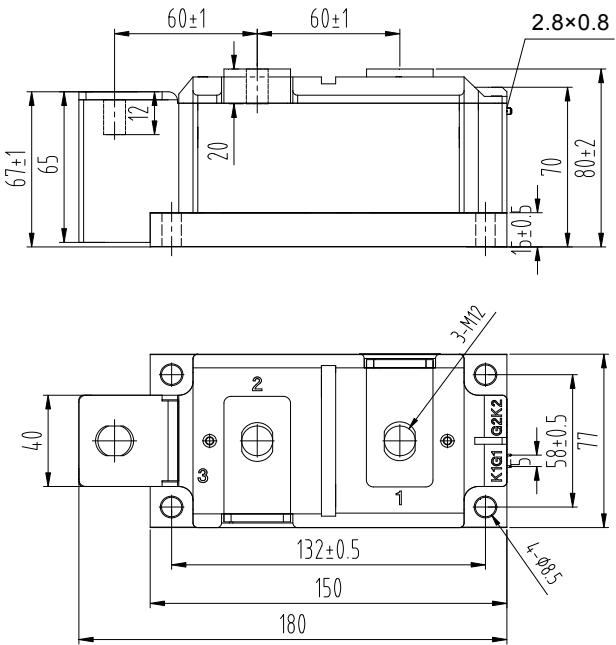
Outline:

Fig. 10

