TECHSEM

H50KPN
PHASE CONTROL THYRISTOR

Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	**850**	**A**
V_{DRM}/V_{RRM}	**4600-5500V**	
I_{TSM}	**12**	**kA**
I^2t	**703**	**10^3A^2S**

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE Min	Type	Max	UNIT
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, T_c=70°C	125			850	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms	125	4600		5500	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			200	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			12	kA
I^2t	I^2t for fusing coordination					703	A^2s*10^3
V_{TO}	Threshold voltage		125			1.07	V
r_T	On-state slope resistance					0.83	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1000A, F=24kN	125			1.90	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			2000	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to 2000A, Gate pulse tr ≤0.5μs I_{GM}＝2.0A	125			150	A/μs
Q_{rr}	Recovery charge	I_{TM}=2000A, tp=2000μs, di/dt=-5A/μs, V_R =50V	125		2500		μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			25		200	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=0.67V_{DRM}	125	0.3			V
$R_{th(j-C)}$	Thermal resistance Junction to case	At 180^0 sine, double side cooled Clamping force 24.0kN				0.022	°C /W
$R_{th(C-h)}$	Thermal resistance case to heatsink					0.005	°C /W
F_m	Mounting force			19	24	26	kN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				560		g
Outline	KT50dT						

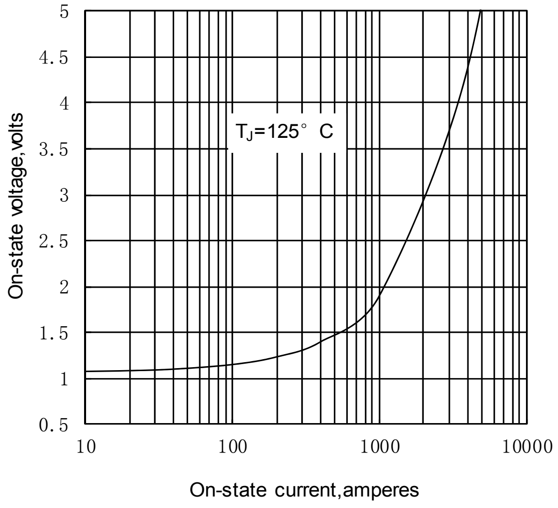
On-state voltage Vs.On-state current

Fig.1

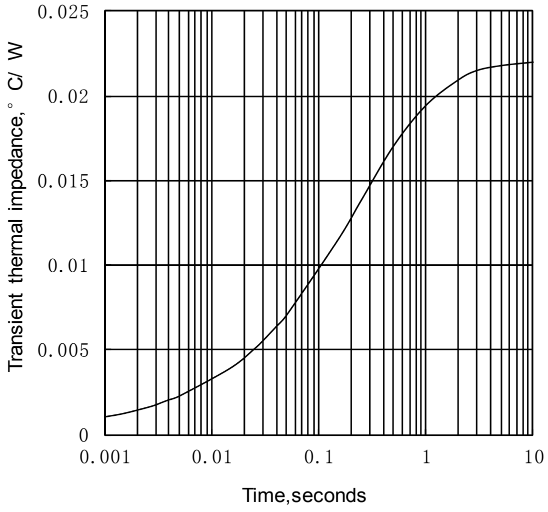
Max. junction to case thermal impedance Vs.time

Fig.2

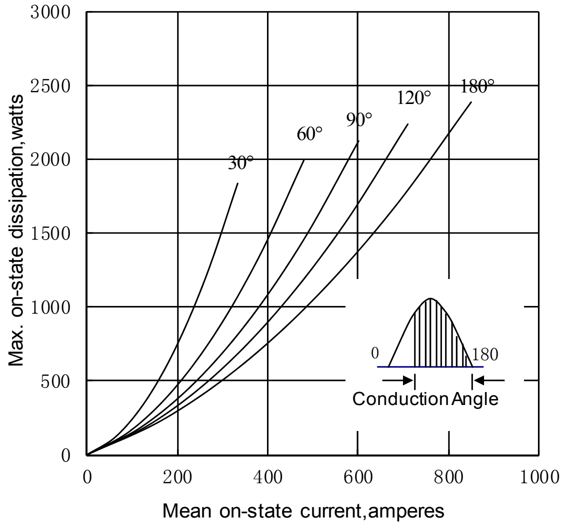
Max. power dissipation Vs.mean on-state current

Fig.3

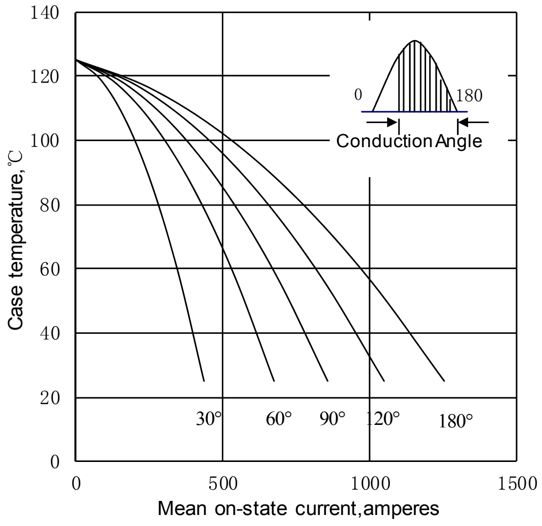
Max.case temperature Vs.mean on-state current

Fig.4

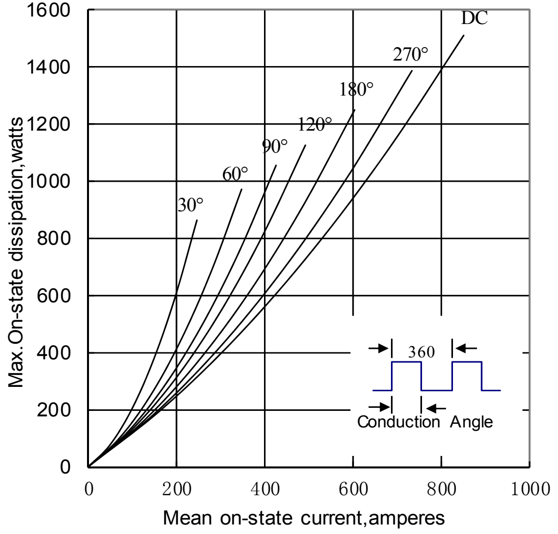
Max. power dissipation Vs.mean on-state current

Fig.5

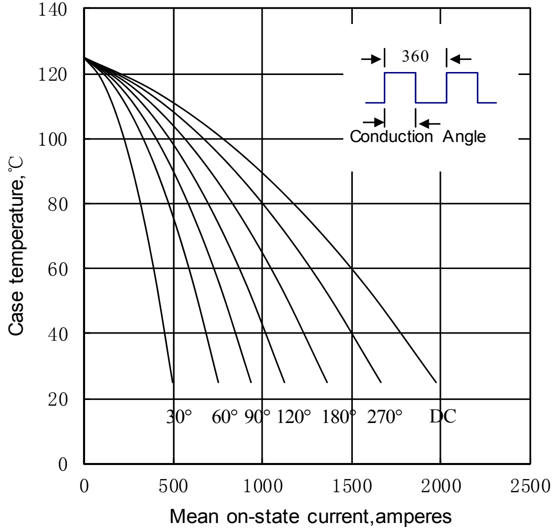
Max. case temperature Vs.mean on-state current

Fig.6

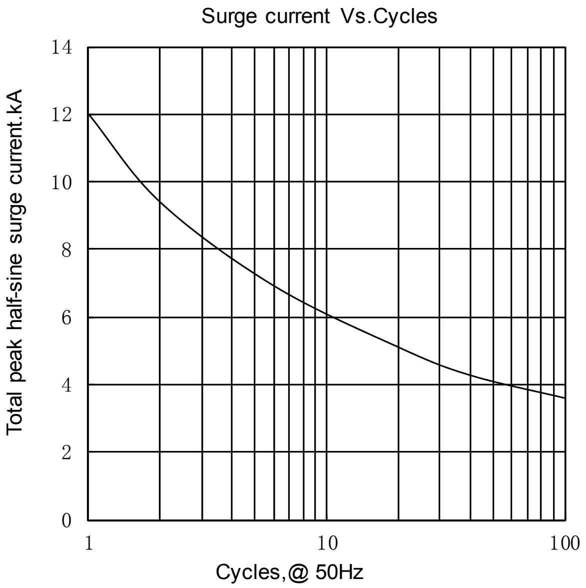
Surge current Vs.Cycles

Fig.7

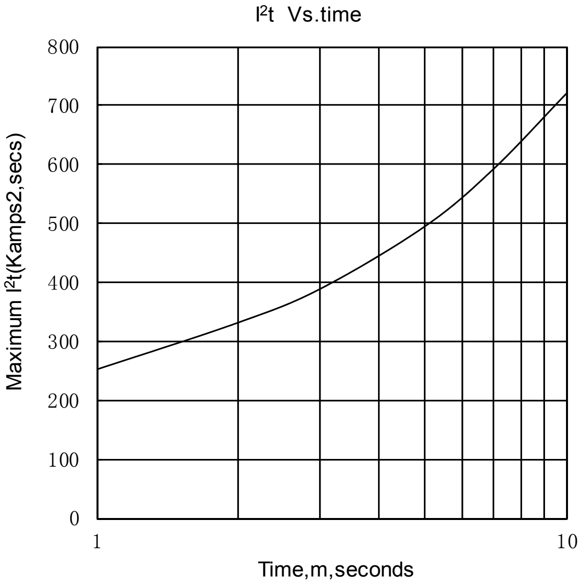
I^2t Vs.time

Fig.8

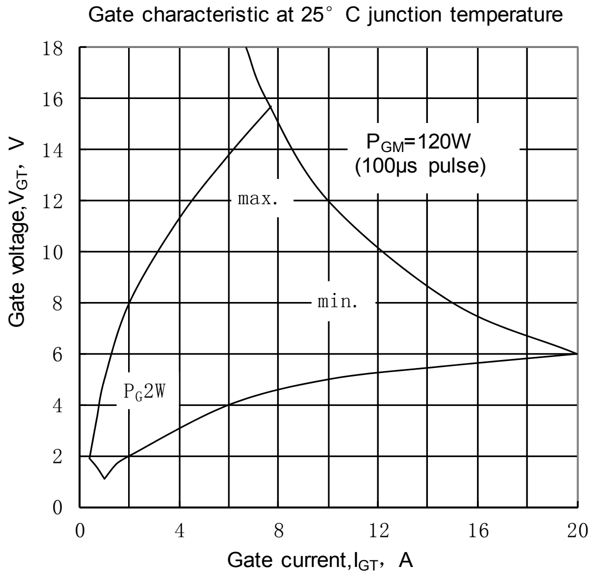
Gate characteristic at 25° C junction temperature

Fig.9

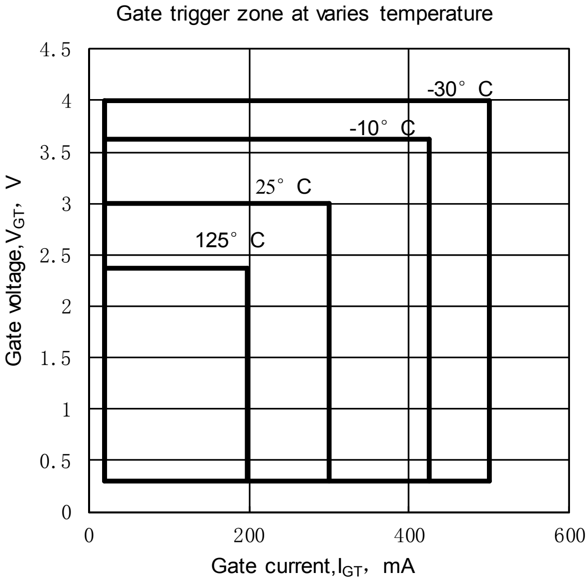
Gate trigger zone at varies temperature

Fig.10

Outline: